REMARKS

Claims 1-10 and 28-36 are pending in this application. No claim has been amended herein.

Claims 1-10 and claims 28-36 have been rejected under 35 U.S.C. §102(e) as being anticipate by newly cited art, Nagai et al., U.S. Publication No. 2002/013412 for reasons stated on pages 2-4 of the Office Action (Paper No. 200040315). As the Examiner has correctly acknowledged, Nagai '412 is Applicants' earlier work product that is also assigned to the same assignee of the instant application. Such a reference only qualifies as prior art against Applicants' claimed invention under 35 U.S.C. §102(e), but **not** as prior art against Applicants' claimed invention under 35 U.S.C. §103© because that subject mater and Applicants' claimed invention "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person." However, as a §102(e) reference, Nagai '412 does **not** disclose key features of Applicants' claims 1-10 and 28-36 as alleged by the Examiner. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections for the following reasons.

Applicants' base claims 1, 5 and 22 define in general a semiconductor device in which a semiconductor element has at least a stress cushioning layer and a semiconductor protective layer, and end faces of these layers are positioned inside the cutting scribe lines formed on a semiconductor wafer, and the range of the surface at the end of the semiconductor element from the end face to the inside of the scribe line is exposed, see page 1, lines 5-15 of Applicants' original disclosure.

As described on page 6, lines 16-25 of Applicants' original disclosure, this arrangement as defined in each of Applicants' base claims 1, 5 and 33 is intended so

as the semiconductor device within an individual dice to withstand the concentrated stress applied at the time of cutting a semiconductor wafer into a plurality of dices and at the time of mounting a semiconductor device in order to minimize damage due to the applied stress and thereby obtaining high reliability and manufacturing yield rate.

Specifically, independent claim 1 expressly defines a semiconductor device comprising:

> "semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line, a stress cushioning layer installed on said semiconductor elements, a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad, external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion, wherein said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have **means for forming each end face on an end surface of said semiconductor elements inside said cutting scribe line** and **exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line**, such that said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."

Likewise, independent claim 5 defines a semiconductor device comprising:

> "semiconductor elements obtained by cutting a semiconductor wafer having an integrated circuit and an electrode pad formed on one side along a cutting scribe line,
> a semiconductor element protective layer installed on said semiconductor elements,
> a stress cushioning layer installed on said semiconductor element protective layer,
> a first opening formed in said semiconductor element protective layer on said electrode pad,
> a second opening formed in said stress cushioning layer on said electrode pad,

a lead wire portion extending to a top of said stress cushioning layer through said first opening and said second opening respectively from said electrode pad,

external electrodes arranged on said lead wire portion on top of said stress cushioning layer, and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes have **means** for **forming each end face on an end surface of said semiconductor elements inside said cutting scribe line** and **exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line**, such that said semiconductor element protective layer, said stress cushioning layer, said lead wire portion, said conductor protective layer, and said external electrodes are located inside of a peripheral edge of said semiconductor elements."

Likewise, independent claim 33 defines a semiconductor device comprising:

at least one semiconductor element including an electrode pad formed on one side along a cutting scribe line;

a stress cushioning layer formed on said semiconductor element;

a lead wire portion extending from said electrode pad to a top of said stress cushioning layer through an opening formed in said stress cushioning layer on said electrode pad;

external electrodes installed on said lead wire portion on top of said stress cushioning layer; and

a conductor protective layer installed on said stress cushioning layer excluding said external electrodes arranged on said lead wire portion,

wherein **each end face of said stress cushioning layer, and said conductor protective layer is formed on an end surface of said semiconductor element so as to be positioned inside said cutting scribe line and to be exposed within a range from said end face on said end surface of said semiconductor element to an inside of said cutting scribe line**.

Again, as expressly defined in each of Applicants' base claims 1, 5 and 33, each end face of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element

protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), is formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line.

This is necessary so that when a semiconductor wafer is to be cut along the cutting scribe line, the semiconductor wafer can be cut without any damage to semiconductor devices within the cutting scribe line due to application of mechanical stress and thermal stress in order to enhance reliability of the semiconductor devices and increase the production yield rate of the semiconductor devices. See pages 9-10 of Applicants' substitute specification.

In contrast to Applicants' independent claims 1, 5 and 33, Nagai '412 discloses a semiconductor device manufacturing method for fabricating semiconductor elements in a specific form mountable in units of wafers 1, as shown in FIG. 3, to achieve subdivision in necessary sizes. According to Nagai '412, a stress relaxation layer is adhered to an IC formation surface, electrode pads, and external electrodes. The stress relaxation layer may be subdivided into a plurality of portions independently in a way corresponding to each conductive layer.

As shown in FIG. 11, the end face of the stress cushioning layer (19) is cut at the same surface on a side which is formed the electrode pad 2 of the semiconductor element.

There is **no** disclosure from Nagai '412 nor is there any teaching or suggestion of the Applicants' claimed "each end face" of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning

layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), [is] formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line, as expressly defined in Applicants' base claims 1, 5 and 33.

Nevertheless, the Examiner cites FIG. 2 of Nagai '412 for allegedly disclosing these key features. However, the Examiner's citation is misplaced. FIG. 2A – FIG. 2F only show major process steps of a method of manufacturing a semiconductor device, as described on paragraph [0050] extending to paragraph [0053], including forming electrode pads 2 and a stress relaxation layer 3 on a wafer 1 and (see FIG. 2A), forming a conductive layer 4 on the stress relaxation layer 3 (see FIG. 2B), filling an epoxy-based liquid sealing resin 5 (see FIG. 2C), laser machining the resultant seal resin layer 5 to define therein cutaway portions to reduce stress forces that can be applied to chips (see FIG. 2D), fabricating ball-like bump electrodes 6 to facilitate electrical interconnection with a mount substrate (See FIG. 2E), and then sub-dividing the wafer 1 into individual pieces to obtain intended semiconductor devices 10. Again, there is **no** disclosure of any cutting scribe line or end faces of any stress cushioning layer or protective layer inside said cutting scribe line as alleged by the Examiner.

The rule under 35 U.S.C. §102 is well settled that anticipation requires that each and every element of the claimed invention be disclosed in a single prior art reference. In re Paulsen, 30 F.3d 1475, 31 USPQ2d 1671 (Fed. Cir. 1994); In re Spada, 911 F.2d 705, 15 USPQ2d 1655 (Fed. Cir. 1990). Those elements must either be inherent or disclosed expressly and must be arranged as in the claim.

Richardson v. Suzuki Motor Co., 868 F.2d 1226, 9 USPQ2d 1913 (Fed. Cir. 1989); Constant v. Advanced Micro-Devices, Inc., 848 F.2d 1560, 7 USPQ2d 1057 (Fed. Cir. 1988); Verdegall Bros., Inc. v. Union Oil Co., 814 F.2d 628, 2 USPQ2d 1051 (Fed. Cir. 1987). The corollary of that rule is that absence from the reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 230 USPQ2d 81 (Fed. Cir. 1986).

The burden of establishing a basis for denying patentability of a claimed invention rests upon the Examiner. The limitations required by the claims cannot be ignored. See In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970). All claim limitations, including those which are functional, must be considered. See In re Oelrich, 666 F.2d 578, 212 USPQ 323 (CCPA 1981). Hence, all words in a claim must be considered in deciding the patentability of that claim against the prior art. Each word in a claim must be given its proper meaning, as construed by a person skilled in the art. Where required to determine the scope of a recited term, the disclosure may be used. See In re Barr, 444 F.2d 588, 170 USPQ 330 (CCPA 1971).

In the present situation, Nagai '412 fails to disclose and suggest key features of Applicants' base claims 1, 5 and 33. Therefore, Applicants respectfully request that the rejection of claims 1-10 and claims 28-36 be withdrawn.

Similarly, claims 1, 3-5, 7-8, 10, 28-31, 33 and 35-36 have been rejected under 35 U.S.C. §102(e) as being anticipate by newly cited art, Shimoishizaka et al., U.S. Patent No. 6,313,532 for reasons stated on pages 4-6 of the Office Action (Paper No. 200040315). Again, contrary to the Examiner's assertion, Shioishizaka '532 does **not** disclose key features of Applicants' claims 1, 3-5, 7-8, 10, 28-31, 33

and 35-36. Therefore, Applicants respectfully request the Examiner to reconsider and withdraw these rejections for the following reasons.

As previously discussed, each of Applicants' base claims 1, 5 and 33 requires that, each end face of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), is formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line. This is necessary so that when a semiconductor wafer is to be cut along the cutting scribe line, the semiconductor wafer can be cut without any damage to semiconductor devices within the cutting scribe line due to application of mechanical stress and thermal stress in order to enhance reliability of the semiconductor devices and increase the production yield rate of the semiconductor devices. See pages 9-10 of Applicants' substitute specification.

In contrast to Applicants' independent claims 1, 5 and 33, Shimoishizaka '532 discloses a conventional semiconductor device manufacturing method for fabricating semiconductor elements, as shown in FIG. 3A - FIG. 3E and FIG. 4A – FIG. 4D, intended to relax stress. According to Shimoishizaka '532, an elastic material layer is formed on the main surface of the semiconductor substrate, so that stress applied to a connection part due to a difference in the coefficient of thermal expansion between a motherboard and the semiconductor device can be absorbed by the elasticity of the elastic material layer.

However, as shown in FIG. 1 of Shimoishizaka '532, the end face of the stress cushioning layer (20) and the conductor protective layer are also cut at the same end face of the semiconductor element.

There is **no** disclosure from Shimoishizaka '532 nor is there any teaching or suggestion of the Applicants' claimed "each end face" of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), [is] formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line, as expressly defined in Applicants' base claims 1, 5 and 33.

Nevertheless, the Examiner seems to cite FIG. 7 of Shimoishizaka '532 for allegedly disclosing these key features. However, the Examiner's citation is misplaced. FIG. 7 is only a perspective view of a semiconductor device including element electrodes arranged in a peripheral portion with a solder resist film partially removed. Again, there is **no** disclosure of any cutting scribe line or end faces of any stress cushioning layer or protective layer inside said cutting scribe line as alleged by the Examiner.

Like Nagai '412, Shimoishizaka '532 also fails to disclose and suggest key features of Applicants' base claims 1, 5 and 33. As a result, Applicants respectfully request that the rejection of claims 1, 3-5, 7-8, 10, 28-31, 33 and 35-36 be withdrawn.

Claims 1, 3, 5, 7, 9, 28-33 and 35 have now been rejected under 35 U.S.C. §103(a) as being unpatentable over newly cited art, Huang, U.S. Patent No. 6,452,270, as modified to incorporate selected features from Yamamoto Tetsuhiro, JP 10-0928654 for reasons stated on pages 7-9 of the Office Action (Paper No. 20040315). However, the Examiner's assertion is factually incorrect and legally improper. Applicants submit that key features of Applicants' claims 1, 3, 5, 7, 9, 28-33 and 35 are **not** disclosed anywhere in Huang '270 and Yamamoto '865, whether taken individually or in combination. As a result, Applicants respectfully request the Examiner to reconsider and withdraw these rejections for the following reasons.

Huang '270, as a primary reference, relates to IC device assembly technology and, more specifically, to solder bump interconnections for mounting chips with copper I/O pads to an interconnection substrate in order to obtain better electrical performance. As shown in FIG. 7, the semiconductor device includes a substrate 310 having a copper contact pad 320; a dielectric layer such as passivation layer 330 formed over the substrate 310; an under bump metallurgy (UBM) 340 consisting of a titanium layer 340a, a first copper layer 340b, a nickel-vanadium layer 340c and a second copper layer 340d; and a solder bump 350 provided on the UBM 340 over the copper contact pad 320 to act as a bump electrode.

As shown in FIG. 8, a dielectric layer 450 is incidentally shown for purposes of forming over the multi-layered lead 440 and the passivation layer 330. However, such a dielectric layer 450 is **not** described in terms of its construction or functionality. More importantly, such a dielectric layer 450 is **not** described, or shown in FIG. 8, in terms of its end face with respect to a cutting scribe line formed on a semiconductor wafer.

As a result, there is **no** disclosure from Huang '270 of any of Applicants' claimed "each end face" of, for example, the stress cushioning layer and the conductor protective layer (see claims 1 and 33), or alternatively, the semiconductor element protective layer, the stress cushioning layer, and the conductor protective layer (see claim 5) on the end face area of the semiconductor element(s), [is] formed so as to be positioned inside the cutting scribe line and to be exposed within a range from the end face of the semiconductor element(s) to an inside of the cutting scribe line, as expressly defined in Applicants' base claims 1, 5 and 33.

As a secondary reference, Yamamoto '865 does **not** remedy the noted deficiencies of Huang '270 in order to arrive at Applicants' base claims 1, 5 and 33. This is because Yamamoto '865 only serves as background art of Applicants' disclosed invention and suffers the same problems inherently associated with Huang '270. Specifically, on page 5, lines 5-12 of Applicants' original disclosure, Applicants cite Yamamoto '865 for disclosing:

> "a semiconductor device of a type in which a resin layer for cushioning stress is installed between external electrodes and semiconductor elements. Individual semiconductor devices are manufactured by processing units of semiconductor wafer in a batch and finally cutting each semiconductor wafer into pieces."

The problem of this type of semiconductor device as described by Yamamoto '865 is that,

> "a plurality of resin layers and external electrodes are formed in units of semiconductor wafers in a batch, and then each semiconductor wafer is cut (diced) into pieces, has a constitution such that the interfaces of a plurality of resin layers sequentially formed on each semiconductor wafer are exposed on the end face of each semiconductor package, so that when a large mechanical stress is applied to the interfaces of the plurality of resin layers at the time of dicing of the semiconductor wafer, **or** when a large thermal stress is applied to the interfaces of the plurality of resin layers due to sudden temperature changes at the time of mounting of the semiconductor package,

> the stress is centralized to the interfaces between the semiconductor element exposed on the end face of the semiconductor package and the plurality of resin layers, so that one or more of the plurality of resin layers are peeled off and the semiconductor package may be damaged.
>
> As mentioned above, such a known semiconductor device cannot always exhibit high reliability, and it is difficult to obtain a high manufacturing yield rate." See pages 5-6 of Applicants' original disclosure.

Because of the problems precisely associated with Yamamoto '865, Applicants propose a solution, a semiconductor device in which a semiconductor element has at least a stress cushioning layer and a semiconductor protective layer, and end faces of these layers are positioned inside the cutting scribe lines formed on a semiconductor wafer, and the range of the surface at the end of the semiconductor element from the end face to the inside of the scribe line is exposed, see page 1, lines 5-15 of Applicants' original disclosure. Again, as discussed previously, Applicants' arrangement is intended so as the semiconductor device within an individual dice to withstand the concentrated stress applied at the time of cutting a semiconductor wafer into a plurality of dices and at the time of mounting a semiconductor device in order to minimize damage due to the applied stress and thereby obtaining high reliability and manufacturing yield rate, see page 6, lines 16-25 of Applicants' original disclosure.

In contrast to Applicants' base claims 1, 5 and 33, Yamamoto '865 only proposes to prevent a semiconductor element with a small number of pins such as a memory, a general-purpose microcomputer, etc., from becoming expensive and the miniaturization rate of QFP from becoming small, even if it is made into CSP (chip size package). See Abstract.

For this purpose, the metallic wiring 14 drawn out of the element electrode 13 of a semiconductor element 12 is made on a first resin layer 15, as shown in FIG.2, and the element electrode 13 of the semiconductor element 12 and a package electrode 11 are electrically connected with each other through the metallic wiring 14. Then, the electric connection with outside is performed at the package electrode 11 positioned in the opening of a second resin layer 10. Moreover, the stress cause by the difference of thermal expansion between a mounting board and the silicon (Si) of the semiconductor element 12 when this semiconductor device and an outside mounting board are mounted is relieved by the polyimide resin layer 17, a first resin layer 15, and a second resin layer 10 made on a passivation film 16. Thus, the chip size package (CSP) can be manufactured at lowcost, because they are processed en block in wafer units without performing individual assembly.

In Yamamoto '865, none of these elements is described in anyway to address the damage due to the concentrated stress applied at the time of cutting a semiconductor wafer and at the time of mounting a semiconductor device, see page 6, lines 16-25 of Applicants' original disclosure. As a result, nowhere in Yamamoto '865 is there any disclosure or suggestion that all the elements in Applicants' claims 1, 5 and 33 are located inside of the peripheral edge of the semiconductor element. This is because typical semiconductor layers are formed across the entire wafer. This is what is shown in FIG. 13 of Yamamoto '865. Specifically, FIG. 13 of Yamamoto '865 shows that all semiconductor devices are within the square or cutting scribe lines. However, all the semiconductor layers constituting those semiconductor devices are still formed across the entire wafer (18). As shown in FIGs. 2-11 and FIGs. 16-22 of Yamamoto '865, all the semiconductor layers,

including, for example, the polyimide resin layer and other resin layers, are formed across the wafer. Only after the resin layers are formed, will the wafer be cut into individual dices. The problem with the approach as disclosed by Yamamoto '865 is that, when the wafer is cut, a large mechanical/temperature stress is applied to the interfaces of the resin layers which, in turn, cause one or more resin layers to peel off and damage the semiconductor devices within each dice. See pages 5-6 of Applicants' original disclosure.

Likewise, nowhere in Yamamoto '865 is there any disclosure of Applicants' claimed "means for forming each end face on an end surface of said semiconductor element inside said cutting scribe line and exposing a range from said end face on said end surface of said semiconductor elements to an inside of said cutting scribe line", as expressly defined in Applicants' base claims 1, 5 and 33.

In order to establish a *prima facie* case of obviousness under 35 U.S.C. §103, the Examiner must show that the prior art reference (or references when combined) must teach or suggest all the claim limitations, and that there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skilled in the art, to modify the reference or to combine reference teachings, provided with a reasonable expectation of success, in order to arrive at the Applicants' claimed invention. The requisite motivation must stem from some teaching or suggestion to make the claimed combination must be found in the prior art, and **not** based on Applicants' disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). See MPEP 2143. In other words, all the claim limitations must be disclosed or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). "All words in a claim must be

considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USQP 494, 496 (CCPA 1970). "Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination." ACS Hospital System, Inc v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). The Examiner must point to something in the prior art that suggests in some way a modification of a particular reference or a combination of references in order to arrive at Applicants' claimed invention. Absent such a showing, the Examiner has improperly used Applicants' disclosure as an instruction book on how to reconstruct to the prior art to arrive at Applicants' claimed invention. Furthermore, any deficiencies in the cited references cannot be remedied with conclusions about what is "basic knowledge" or "common knowledge". See In re Lee, 61 USPQ 2d 1430 (Fed. Cir. 2002).

In the present situation, both Huang '270 and Yamamoto '865 fail to disclose and suggest key features of Applicants' base claims 1, 5 and 33. Therefore, in view of the foregoing explanations and inherent deficiencies of Huang '270 and Yamamoto '865, Applicants respectfully request that the rejection of claims 1, 3, 5, 7, 9, 28-33 and 35 be withdrawn.

Lastly, dependent claims 2, 6 and 34 have also been rejected under 35 U.S.C. §103(a) as being unpatentable over Huang, U.S. Patent No. 6,452,270, as modified to incorporate selected features from Yamamoto Tetsuhiro, JP 10-0928654, and Okada et al., U.S. Patent No. 6,111,317 for reasons stated on pages 10-12 of the Office Action (Paper No. 20040315). Since the rejection is predicated upon the correctness of the rejection of base claims 1, 5 and 33, Applicants respectfully

traverse this rejection for the same reasons discussed against the rejection of base claims 1, 5 and 33. Moreover, Applicants also note that Okada '317 only shows construction of a tip/passivation film/lead/barrier metal/external electrode/ semiconductor protective layer, and does **not** show or describe the use of a stress cushioning layer. As a result, the idea of a position relation between the stress cushioning layer and the semiconductor protective layer as described in Applicants' claims 2, 6 and 34 is **not** described or suggested in view of Okada '317.

In view of the foregoing amendments, arguments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. Should any questions remain unresolved, the Examiner is requested to telephone Applicants' attorney at the Washington DC area office at (703) 312-6600.

INTERVIEW:

In the interest of expediting prosecution of the present application, Applicants respectfully request that an Examiner interview be scheduled and conducted. In accordance with such interview request, Applicants respectfully request that the Examiner, after review of the present Amendment, contact the undersigned local Washington, D.C. area attorney at the local Washington, D.C. telephone number (703) 312-6600 for scheduling an Examiner interview, or alternatively, refrain from issuing a further action in the above-identified application as the undersigned attorneys will be telephoning the Examiner shortly after the filing date of this Amendment in order to schedule an Examiner interview. Applicants thank the Examiner in advance for such considerations. In the event that this Amendment, in

and of itself, is sufficient to place the application in condition for allowance, no Examiner interview may be necessary.

To the extent necessary, Applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage of fees due in connection with the filing of this paper, including extension of time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, No. 01-2135 (Application No. 503.39864X00), and please credit any excess fees to said deposit account.

Respectfully submitted,

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